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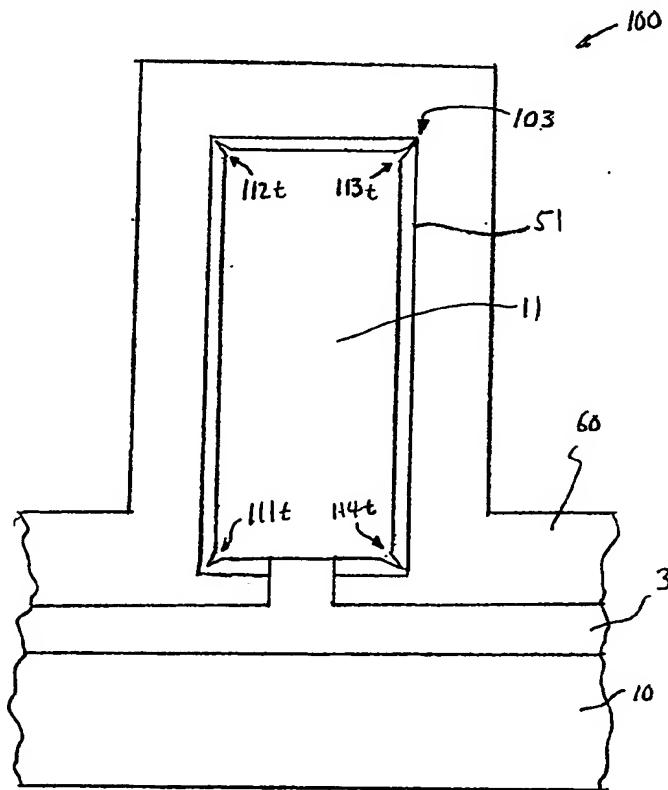
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## (54) Title: INTEGRATED ANTIFUSE STRUCTURE FOR FINFET AND CMOS DEVICES



(57) Abstract: A method is described for fabricating an antifuse structure (100) integrated with a semiconductor device such as a FINFET or planar CMOS device. A region of semiconducting material (11) is provided overlying an insulator (3) disposed on a substrate (10); an etching process exposes a plurality of corners (111-114) in the semiconducting material. The exposed corners are oxidized to form elongated tips (111t-114t) at the corners; the oxide (31) overlying the tips is removed. An oxide layer (51), such as a gate oxide, is then formed on the semiconducting material and overlying the corners; this layer has a reduced thickness at the corners. A layer of conducting material (60) is formed in contact with the oxide layer (51) at the corners, thereby forming a plurality of possible breakdown paths between the semiconducting material and the layer of conducting material through the oxide layer. Applying a voltage, such as a burn-in voltage, to the structure converts at least one of the breakdown paths to a conducting path (103, 280).



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